Remarks

The Examiner objected to certain typographical or other errors which were not properly identified in the specification or drawings. The Applicants have amended the Specification to correct these errors. The Examiner pointed out that in claim 18 "said plurality of rails" lacked a proper antecedent. Claim 18 has been amended to delete "plurality of" to provide the necessary antecedent. No new matter has been added by this amendment.

Claim Rejections - 35 U.S.C. § 102

The Examiner rejected under 35 U.S.C. 102(b) as being anticipated by Burns, Jr. et al. (6,077,745). The Examiner indicated that Burns Jr. et al, figures 1-72, and related text on col. 1-34 (figures 129, 10, 11, 26,37), disclose a method of forming a memory cell, comprising: forming rails/pillars 230 of semiconductor material on a substrate 235; doping a first portion of said rails (see figure 37); forming a dielectric 460 on said first portion of at least every other one of said rails; forming a plate electrode 265 (see figure 10) on said first portion adjacent pairs 230 of said rails; forming an FET 205 in a second portion of said rails adjacent said first portion, said FET having a gate electrode 275 disposed on all exposed sides of a part of said second portion of said rails.

The applicants wish to point out that the construction and operation taught and described by Burns Jr. et al. is quite different than the present invention. In particular, the pillars 230 in Burns are not the same as rails. (12A and 12B) in the subject application.

The pillars 230 in Burns Jr. et al. are used to construct vertical FETs with source/drain at the tops and bottoms of the silicon pillars and must be kept laterally short (pillar-like) and as a result, in contrast to our rails in which sources and drains are placed horizontally along the rails. Even more striking is the fact that the pillars do not contain both the source and drain, with the lower of the two in the bulk silicon surrounding the pillar, in contrast to our rails which completely contain both source and drain. A third point is that the pillars do not provide a means of establishing a source/drain that is both mostly isolated from the substrate and in contact with a storage capacitor, in contrast to our rails which do.

The Examiner considers the floating gate 265 of Burns Jr. et al. as equivalent of our plate electrode, however, the floating gate of Burns Jr. et al. is in no way equivalent to our plate electrode. Our plate electrode is a conductor which serves as a portion of our storage capacitor while the floating gate 265 of Burns Jr. et al. forms a gate which stores charge to change the threshold voltage. Thus Burns Jr. et al. does not form a plate electrode on the pillar.

It should be understood that the gate electrode 275 of Burns Jr. et al. is not disposed on the sides of a part of said second portion of their pillar for two reasons. First, it is adjacent to the floating gate 265, not the pillar 230. Second, it is on the first portion of the pillar where the floating gate 265 is disposed, not on a second portion of the pillar.

Accordingly, Burns Jr. et al. does not suggest or teach the method of claim 17. It is respectfully submitted that claim 17 and all claims depending on claim 17, namely, claims 18-20 are allowable under 35 U.S.C. § 102(b).

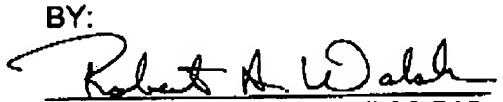
Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Jeffrey S. Brown, et al.

BY:



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